Circuitry analyses by using high quality image acquisition and multi-layer image merge technique

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ABSTRACT

By using high quality image acquisition and multi-layer image merge technique, a novel technique of IC circuitry analysis has been developed and successfully applied to more than 50 industrial products analysis in one year. A series of in-house designed software ensures the successful rate to be up to 95% and the total working time to be less than 2 months for analog/mix-signal ICs of any scale and typically 10~100K gates counts digital devices. The software environment was also featured by multiple language, multiple users accessible, project teamwork feasible, TCL script extension support, automatic backup/restore, and GUI based in Windows, Linux, and UNIX platform.

INTRODUCTION

Circuitry analysis was commonly employed when doing strategic planning of technology development, project feasibility study, cost evaluation, project debugging, benchmark study, and patent claims analysis. However, with the evolution of IC process technology, device scaling down enhanced the complexity of circuitry and the number of transistors increased exponentially. It is getting more difficult to analyze IC circuits by simply personal handicraft without automation tools and standard process flow. It will require tremendous engineering efforts to figure out the whole design.

A successful circuit analysis require excellent techniques of sample preparation (de-processing) and circuit analysis, we have achieved significant break-through of all mandatory technologies in these two areas, including decap, delayer, automatic image acquisition, high precision stitching and alignment of the images of different layers, automatic layout/netlist extraction, intelligent circuit analysis assistant, and result integrality check (ERC, LVS, DRC).

In this report, the in-house developed software was aimed to increase the controllability, shorten the delivery time of the project, and reduce the work load and mental intension during circuitry analyses. Meanwhile, a standard process flow of reverse engineering was characterized by highly automatic chip imaging process, efficient/effective layout recognition capability, precise circuitry extraction and real-time layout-netlist-schematic verification capability.

EXPERIMENTAL

The work flow of circuit reverse engineering was shown in Fig 1. The project was commenced by decap and delayering of IC chips. Wet chemical etching, parallel lapping, CMP (chemical mechanical polishing), RIE (reactive ion etch) and ICP (ion coupled plasma) were conducted interchangeably to do the material removal for the layer-by-layer chip imaging. The chip images are captured by either optical microscope (OM) or scanning electron microscope (SEM) equipped with customized stage and digital camera, which enable the efficient image acquisition by auto-stepping of electronic stage.

The images were then processed by in-house designed software to eliminate image distortion and sample leaning, to ensure seamless image stitching in one layer, and to precisely align among multiple layers. The image recognition and 3D array error disperse algorithm are employed in achieving the perfect result.

By integrating multi-layer images, simplified layout and netlist can be traced out automatically by cell definition, cell/path/via image recognition and data verification. Different work flows and tools are designed for analog and digital circuit tracing respectively.

The hierarchical schematics build-up and block diagram extraction are done interactively with engineering efforts – the software provides hints and suggestions of the device grouping and block boundary, quickly generate the schematics of the partial netlist for the engineers to inspect. Consequently, engineers judge and define the functional blocks. And then, the software will search/replace the defined blocks, rebuild symbol, netlist, and schematics automatically, and repeat the process until the whole block/schematic diagram was created..

RESULTS AND DISCUSSION

This novel technique of circuitry analysis has been applied to a variety of industrial products, including ADC/DAC IC, LCD/OLED driver IC, RF IC, consumer IC, power management IC, video processor and clock/PLL IC etc. Both analog and digital circuits could be investigated successfully. For those ICs with minimal line width of 0.25μm and larger, optical microscope with visible light source was employed to do the image acquisition. For those ICs with minimal line width of 0.13-0.22μm, optical microscope with UV light shall be employed. While for ICs of 0.13μm and downward, field emission SEM will be a must to achieve reasonable resolution and working time for layout recognition.

Automatic photo imaging process was a key point to reduce the laboring of image acquisition. Auto-stepping control of the 5-axis electronic stage was a crucial attachment with the ability of auto focusing. High speed, high resolution 3-CCD camera was another key part to ensure the image quality. The image acquisition time of visible light imaging was controlled to be less than 4 sec for every shot, including the stepping time, auto focusing, and auto leveling of the electronic stage. The UV exposure takes longer time – around 10 sec per shot. The SEM system requires customized electron beam source, which is able to shorten the SEM imaging time within 5 sec per shot. Fig.2, 3 and 4 are the installed visible light optical system, UV light system and SEM system.

It was known that higher magnification of the imaging would result in smaller view size, which would thus increase the total number of images of a certain size of IC chips. Ultimately, for die size >50 mm^2, more than 10K photos would be generated by 1000X magnification. It will thus take about 10 hrs for a photo imaging job. So, the non-critical layers, such as the top metal layers and active layer will be imaged at lower magnification, 200X or 500X, to save the working time. Generally speaking, decap, delayer, and imaging process of most of IC chips, up to 7-8 metal layers, could be done in 1-2 weeks. The stitching and alignment jobs can be conducted in parallel with the image acquisition. The automation level is quite high and the human involvement is not that much. The variation of stitching and alignment error is well controlled to be less than 1/2 of the minimal line width.

By integrating all photo images and well-align every different layers, the self-developed software provided versatile functions to view the die images, including zoom-in, zoom-out, pan, split windows, and dock able windows, as shown in Fig.5 and 6. In addition, two neighboring layers (say, M4 and M3, or M2 and M1, etc.) can be combined and displayed in parallel. Besides, the transparency of images is adjustable between these two layers. Therefore, it is possible to cite all related layers at one time for engineering study. These functions can be applied to layout recognition process as well, as shown in Fig.7. Overlapped multi-layer layout and image-to-layout are very easy to manipulate on screen, which ensures an efficient and effective operation of the layout analysis.

However, the most time consuming part and knowledge intensive part shall be circuitry analysis, the self developed software provides lots of tools to help engineer to fulfill the task. It went through image recognition, layout annotation, and devices/hierarchy schematics extraction; lots of automatic jobs are done through the TCL scripts library during all these process. The full report would be done, until all cell blocks and cell symbols were generated and electrical rule check (ERC) was conducted automatically, as shown in Fig.8. The analytical results could be provided in standard formats, such as GDSII, CIF, EDIF, SPICE, Verilog, VHDL, PDF, etc., and the format of self-developed EDA software with better capability of viewing all die images, layout, and schematics.

It was also characterized by a fancy feature of cross reference between schematics and layout, and/or, between schematics and die images, as shown in Fig.9. This function is an important feature of this software, which could be applied to product debugging for failure diagnostics too. Although the circuit tracing process is quite automatic with the aid of the self-developed software, engineering intelligence is still mandatory to verify the correctness of the extraction results. In order to precisely manage the engineering process, this software also possesses the ability to record the whole circuit tracing history in background automatically. It provides the means of calling back the history data at any time. Besides, it enables the project management to every single step.

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SUMMARY

Circuitry analysis is a challenging job for nowadays IC products. Automatic tools, integrated hardware and software, shall be very crucial for an efficient and effective study. The novel technique developed in this work makes ease of the job and save tremendous engineering efforts, and already being applied very successfully in many cases. Besides, the efficiency has been improved 2~20 times, compared to that of traditional way.

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Figures and Photos

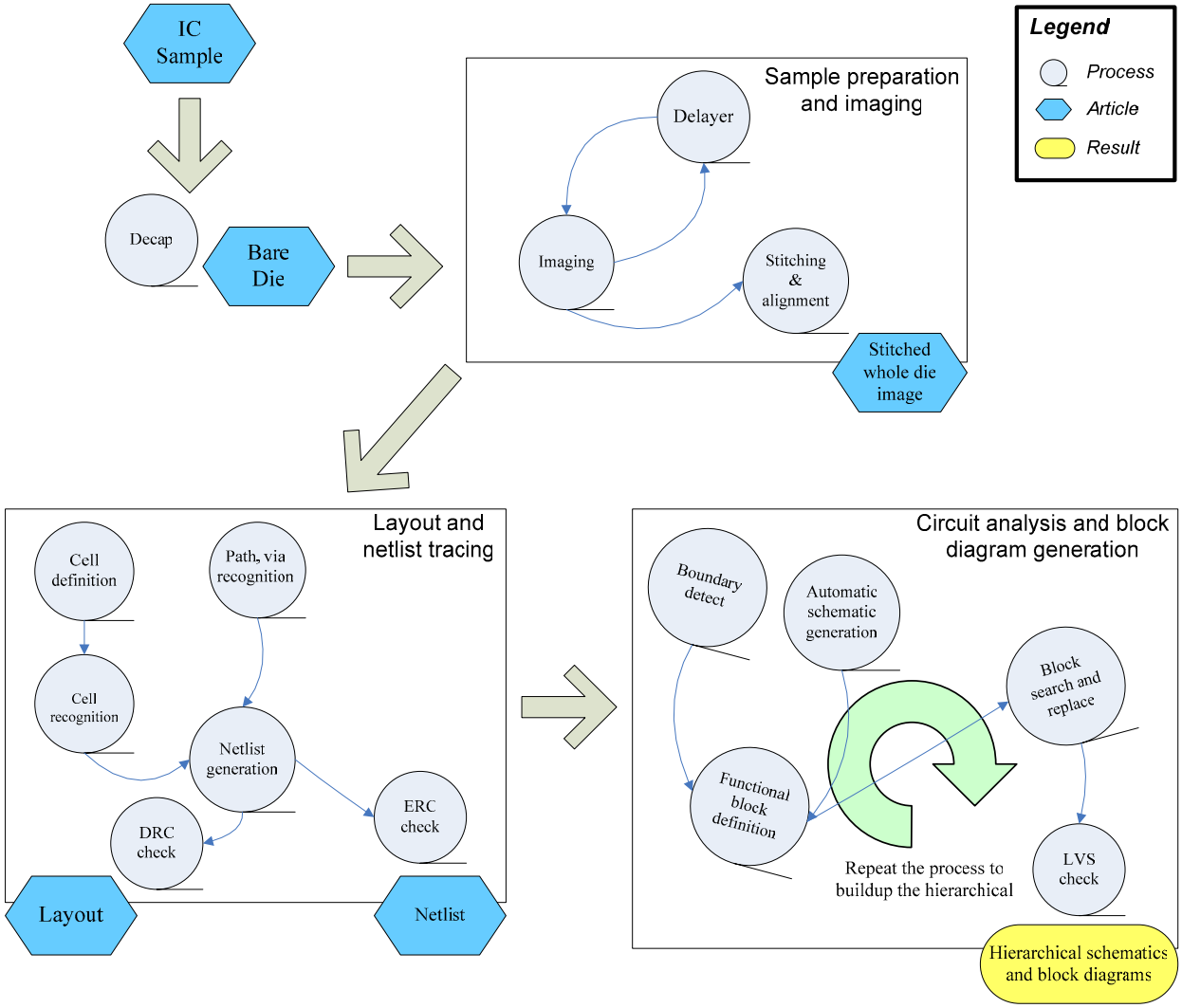


Fig.1The work flow of the circuitry analysis

Fig 2 Visible light system

Fig 3 UV light system

Fig 4 SEM system

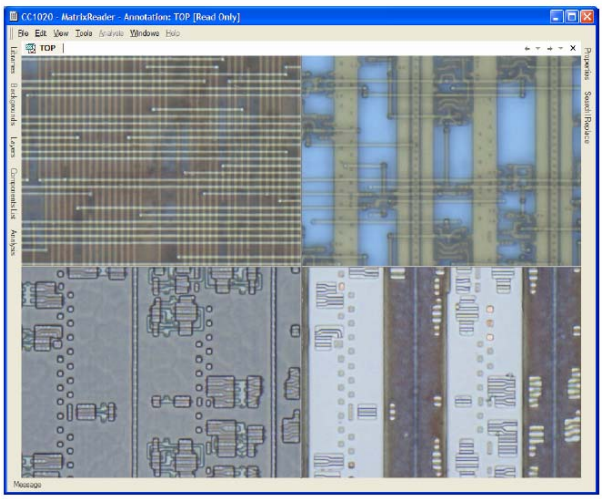


Fig.5 The image viewing software allows die images to be examined by split window in many different ways.

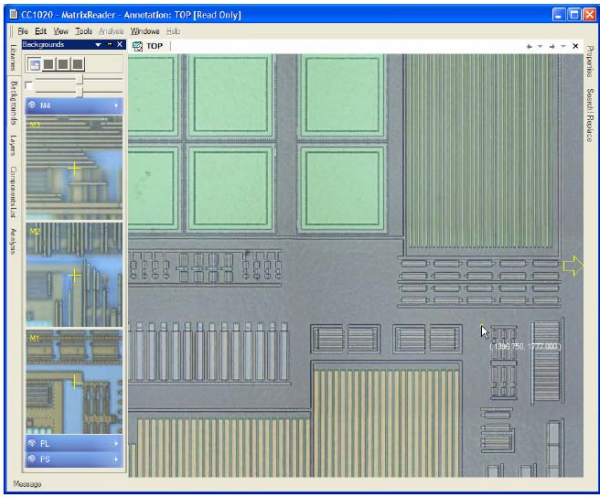


Fig.6 The image viewing software also provides dock-able windows to check multi-layer images quickly.

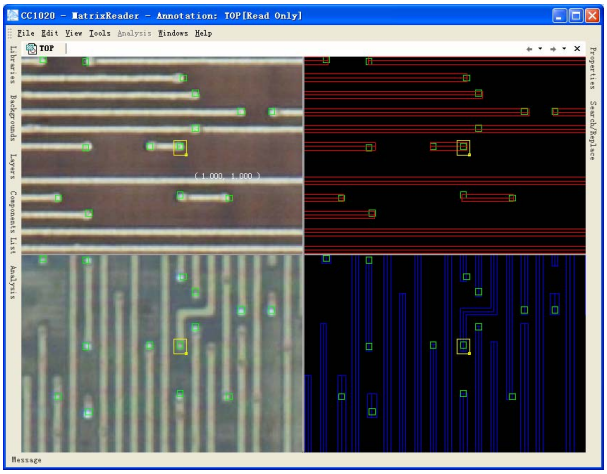
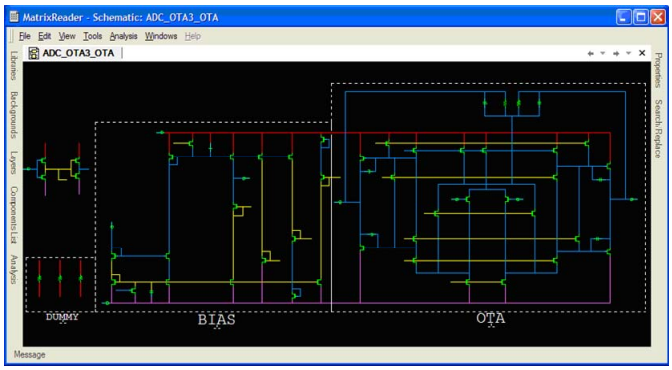


Fig.7 Layout recognition



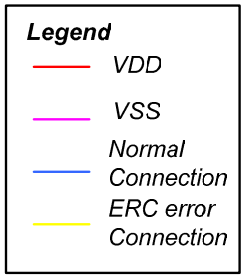


Fig.8 Real time ERC check

Fig.9 Illustration the ability of cross reference between layout and schematics